CLAIMS

1. A memory cell comprising a variable resistive element and a current control element controlling a current flowing in said variable resistive element, wherein said current control element is a Schottky diode.

2. The memory cell as set forth in claim 1, wherein a first electrode of said Schottky diode is a polycrystalline silicon region selectively formed in said insulating film, and a second electrode of the same is a metal film deposited on said polycrystalline silicon region.

3. The memory cell as set forth in claim 2, wherein said Schottky diode has a Schottky barrier between said polycrystalline silicon region and a metal silicide film formed between said polycrystalline silicon region and said metal film.

4. The memory cell as set forth in claim 1, wherein said variable resistive element is formed of a resistive material having a perovskite-type crystalline structure.

5. The memory cell as set forth in claim 4, wherein a first electrode of said Schottky diode is a polycrystalline silicon region selectively formed in said insulating film, and a second electrode of

the same is a metal film deposited on said polycrystalline silicon region.

6. The memory cell as set forth in claim 5, wherein said Schottky diode has a Schottky barrier between said polycrystalline silicon region and a metal silicide film formed between said polycrystalline silicon region and said metal film.

7. The memory cell as set forth in claim 4, wherein a first electrode of said Schottky diode is a second conductive type impurity region formed on a first conductive type semiconductor substrate, and a second electrode of the same is a metal film deposited on said impurity region.

8. The memory cell as set forth in claim 7, wherein said semiconductor substrate is a silicon substrate, and said Schottky diode has a Schottky barrier between said impurity region and a metal silicide film formed between said impurity region and said metal film.

9. The memory cell as set forth in claim 8, wherein said impurity region is selectively formed in an element isolation region formed in said semiconductor substrate.

10. The memory cell as set forth in claim 9, wherein a

variable resistive film constituting said variable resistive element is deposited on said second electrode of said Schottky diode by a self-aligning manner.

11. A memory device in which memory cells are located at positions where word lines and bit lines arranged in a matrix intersect with each other, wherein

said memory cell is constituted by a series circuit including a variable resistive element and a Schottky diode controlling a current flowing in said variable resistive element, and

one end of said series circuit is connected to said word line, and other end of the same is connected to said bit line, respectively.

12. The memory device as set forth in claim 11, wherein said word line is constituted by a polycrystalline silicon region selectively formed in an insulating film.

13. The memory device as set forth in claim 12, wherein said first electrode of said Schottky diode is said polycrystalline silicon region, and said second electrode of the same is a metal film deposited on said polycrystalline silicon region.

14. The memory device as set forth in claim 13, wherein said Schottky diode has a Schottky barrier between said polycrystalline silicon region and a metal silicide film formed between said

polycrystalline silicon region and said metal film.

15. The memory device as set forth in claim 11, wherein said variable resistive element is formed of a resistive material having a perovskite-type crystalline structure.

16. The memory device as set forth in claim 15, wherein said word line is constituted by a polycrystalline silicon region selectively formed in an insulating film.

17. The memory device as set forth in claim 16, wherein said first electrode of said Schottky diode is said polycrystalline silicon region, and said second electrode of the same is a metal film deposited on said polycrystalline silicon region.

18. The memory device as set forth in claim 17, wherein said Schottky diode has a Schottky barrier between said polycrystalline silicon region and a metal silicide film formed between said polycrystalline silicon region and said metal film.

19. The memory device as set forth in claim 15, wherein

a first electrode of said Schottky diode is connected to said word line,

a second electrode of said Schottky diode is connected to one end of said variable resistive element, and

said other end of said variable resistive element is connected to said bit line.

20. The memory device as set forth in claim 19, wherein said word line is constituted by an impurity region selectively formed in an element isolation region formed in said semiconductor substrate.

21. The memory device as set forth in claim 20, wherein said first electrode of said Schottky diode is said impurity region, and a second electrode of the same is a metal film deposited on said impurity region.

22. The memory device as set forth in claim 21, wherein said semiconductor substrate is a silicon substrate, and said Schottky diode has a Schottky barrier between said impurity region and a metal silicide film formed between said impurity region and said metal film.

23. The memory device as set forth in claim 22, wherein a variable resistive film constituting said variable resistive element is deposited on said second electrode of said Schottky diode by a self-aligning manner.

24. A manufacturing method of forming a memory cell constituted by a series circuit of a variable resistive element and a

Schottky diode, on a semiconductor substrate, comprising steps of:

forming an insulating film having openings on which impurity regions formed on one surface of said semiconductor substrate are exposed;

depositing a metal film constituting an electrode of said variable resistive element in said openings of said insulating film;

depositing a variable resistive film constituting a resistor of said variable resistive element on said metal film; and

forming a Schottky diode by forming a metal silicide film between said impurity region and said metal film by a heat treatment.

25. The manufacturing method as set forth in claim 24, wherein said variable resistive film is deposited on said metal film in said opening by a self-aligning manner.

26. The manufacturing method as set forth in claim 25, wherein a temperature of said heat treatment is a temperature capable of improving a crystalline property of said variable resistive film.

27. The manufacturing method as set forth in claim 26, wherein

said semiconductor substrate is a silicon substrate, and

said Schottky diode has a Schottky barrier between said metal

silicide film and said impurity region.

28. The manufacturing method as set forth in claim 27, wherein said metal film is formed of a refractory metal material.

29. The manufacturing method as set forth in claim 28, wherein said refractory metal material is selected from at least one of Pt, Ti, Co and Ni.

30. A manufacturing method of forming a memory cell constituted by a series circuit of a variable resistive element and a Schottky diode, on a semiconductor substrate, comprising steps of:

forming an insulating film having openings on which impurity regions formed on one surface of said semiconductor substrate are exposed;

depositing a metal film constituting an electrode of said variable resistive element in said openings of said insulating film;

depositing a variable resistive film having a first film thickness and constituting a resistor of said variable resistive element on said metal film;

forming a Schottky diode by forming a metal silicide film between said impurity region and said metal film by a heat treatment, and

depositing a variable resistive film having a second film thickness and constituting said resistor on said variable resistive film

having said first film thickness.

31. The manufacturing method as set forth in claim 30, wherein a temperature of said heat treatment is a temperature capable of improving a crystalline property of said variable resistive film having said first film thickness.

32. The manufacturing method as set forth claim 31, wherein

said semiconductor substrate is a silicon substrate, and

said Schottky diode has a Schottky barrier between said metal silicide film and said impurity region.

33. The manufacturing method as set forth in claim 32, further comprising a step of further performing a heat treatment after deposition of said variable resistive film having said second film thickness,

wherein a temperature of said heat treatment is a temperature capable of improving a crystalline property of said variable resistive film having said second film thickness and capable of reducing a resistance value of said metal silicide film.

34. The manufacturing method as set forth in claim 33, wherein said metal film is formed of a refractory metal material.

35. The manufacturing method as set forth in claim 34, wherein said refractory metal material is selected from at least one of Pt, Ti, Co and Ni.

36. A manufacturing method of forming a memory cell constituted by a series circuit of a variable resistive element and a Schottky diode, on a semiconductor substrate, comprising steps of:

selectively forming a polycrystalline silicon region in an insulating film formed on one surface of said semiconductor substrate;

depositing a metal film constituting an electrode of said variable resistive element on said polycrystalline silicon region;

depositing a variable resistive film constituting a resistor of said variable resistive element on said metal film; and

forming a Schottky diode by forming a metal silicide film between said polycrystalline silicon region and said metal film by a heat treatment.

37. The manufacturing method as set forth in claim 36, wherein a temperature of said heat treatment is a temperature capable of improving a crystalline property of said variable resistive film.

38. The manufacturing method as set forth claim 37, wherein said Schottky diode has a Schottky barrier between said

metal silicide film and said polycrystalline silicon region.

39. The manufacturing method as set forth in claim 38, wherein said metal film is formed of a refractory metal material.

40. The manufacturing method as set forth in claim 39, wherein said refractory metal material is selected from at least one of Pt, Ti, Co and Ni.

41. A manufacturing method of forming a memory cell constituted by a series circuit of a variable resistive element and a Schottky diode, on a semiconductor substrate, comprising steps of:

selectively forming a polycrystalline silicon region in an insulating film formed on one surface of said semiconductor substrate;

depositing a metal film constituting an electrode of said variable resistive element on said polycrystalline silicon region;

depositing a variable resistive film having a first film thickness and constituting a resistor of said variable resistive element on said metal film;

forming a Schottky diode by forming a metal silicide film between said polycrystalline silicon region and said metal film by a heat treatment; and

depositing a variable resistive film having a second film thickness and constituting said resistor on said variable resistive film

having said first film thickness.

42. The manufacturing method as set forth in claim 41, wherein a temperature of said heat treatment is a temperature capable of improving a crystalline property of said variable resistive film having said first film thickness.

43. The manufacturing method as set forth claim 42, wherein said Schottky diode has a Schottky barrier between said metal silicide film and said polycrystalline silicon region.

44. The manufacturing method as set forth in claim 43, further comprising a step of further performing a heat treatment after deposition of said variable resistive film having said second film thickness,

wherein a temperature of said heat treatment is a temperature capable of improving a crystalline property of said variable resistive film having said second film thickness and capable of reducing a resistance value of said metal silicide film.

45. The manufacturing method as set forth in claim 44, wherein said metal film is formed of a refractory metal material.

46. The manufacturing method as set forth in claim 45, wherein said refractory metal material is selected from at least one of

Pt, Ti, Co and Ni.